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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,531	07/31/2006	Raymond J. Grover	PHGB03 0081 US	9882

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Intellectual Property and Licensing
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EXAMINER	
ULLAH, ELIAS	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
10/03/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/561,531	GROVER, RAYMOND J.	
	Examiner	Art Unit	
	ELIAS M. ULLAH	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-9* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-9* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *19 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/19/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "termination structure surrounding the active area" i.e. termination structure 16 in claims 1 and 8 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claims 1 and 8 recite " the trenches, gate electrodes and layer of gate insulating material of the lateral devices being formed in the same respective process steps as trenches, insulated electrodes.." However, it is not clear what are the process steps are referring as "same process steps" in order to consider the claimed limitations. Further, "same process" may not be possible since gate electrode is typically conductor and gate insulating layer is typically oxide. For purpose of examination, the recited claim limitations "same process step" will read as whatever steps are used in the references to form "gate electrode, gate insulating materials ..."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams et al. (Williams, Us 2002/0168821).

With regard to claim 1, Williams shows a semiconductor device having a semiconductor body (267 in Fig. 23) comprising an active area (260) and a termination structure (290) surrounding (continuous process of Fig.23 will surround the active area) the active area (260), the termination structure comprising a plurality of lateral trench gate transistor devices (see Fig. 23, i.e. wherein elements 292 and 293 are located) connected in series (see Fig. 23) and extending from the active area (260) towards a peripheral edge (edge of element 267) of the semiconductor body (267), each lateral device comprising a trench having a gate electrode (293) therein separated from semiconductor body (267) by a layer of gate insulating material (261), the trenches (wherein 293 and 294 are located in Fig. 23), gate electrodes (293 and 294) and layers of insulating material of the lateral devices (see Fig. 23) formed in the same respective process steps (process limitation the product claims "product-by-process" see MPEP 2113) as trenches, insulated electrodes therein and layers of material insulating the insulated electrode of devices in active area (see Fig. 23 under active area 260), the gate electrode of the lateral devices extending through a region of a first conductively type (Nepi in Fig. 23) and part way through an underlying region of a second opposite conductivity (P_B in Fig. 23), with each lateral device including an electrically conductive connection (303) between its gate electrode (293) and the first conductivity type region (Nepi) at the side of the lateral device closer to the active area (260) such that a voltage difference (functional of the active devices) between the active area (260) and the peripheral edge is distributed across the lateral devices (see Fig. 23 this is intended use of the structure).

With regard to claim 2, Williams shows a semiconductor device wherein the active area (260) comprises devices having a region of the first conductivity type (Nepi in Fig. 23) which is formed in the same process as the first conductivity typed region of the lateral device (see Fig. 23, and further process limitation the product claims "product-by-process" see MPEP 2113).

With regard to claim 3, Williams shows a semiconductor device wherein the insulated electrodes of the active area devices are gate electrodes (266) of trench gate transistor device (see Fig. 23 wherein 266 are located) and the first conductivity region (Nepi) of the active area device form a channel accommodation region (P_B in Fig. 23).

With regard to claim 4, Williams shows a semiconductor device wherein insulated electrodes (264 or 293) of the active area (260) devices are trenched electrode (264 or 293) of schottky rectifiers (wherein trenched electrode of 264 is capable of act as Schotky rectifiers electrode)

With regard to claim 5, Williams shows a semiconductor device wherein the layer of insulating material (261) is thicker over the bottom of the trenches of the lateral devices than over at least a portion of the sidewalls of the said trenches (see Fig. 23 wherein electrode 293 causes portion of insulating layer i.e. sidewall to thin).

With regard to claim 6, Williams shows a semiconductor device wherein the doping level of a respective portion of the region second conductivity adjacent the bottom of each of gate trenches of the lateral devices is higher than that of reminder of the second conductivity type region (see paragraph [0137] wherein doping is near bottom trench is lighter).

With regard to claim 7, Williams shows a semiconductor device wherein the semiconductor body (267) is rectangular in plane of the body (see Fig. 23) and the connection (303) are provided towards on or more corner of the body (see Fig. 23).

With regard to claim 8, Williams shows a method semiconductor device having a semiconductor body (267 in Fig. 23) comprising an active area (260)and a termination structure (290) surrounding (continuation process of Gig. 23 will comprises additional termination area and will surrounding the active area) the active area (260), the termination structure comprising a plurality of lateral trench-gate transistor devices (wherein 293 and 294 are located in Fig. 23) connected in series (see Fig. 23) and extending from the active area (260) towards a peripheral edge (edge of element 267) of the semiconductor body (267), each lateral device comprising a trench (wherein 293 and 294 are located in Fig. 23) having a gate electrode (293 and 294) therein separated from the semiconductor body (267) by a layer of gate insulating material (261) the gate electrodes of the lateral devices extending through a region of a first conductivity type (Nepi) and part way through an underlying region (P_B) of a second, opposite conductivity type (p –type), with each lateral device including an electrically conductive connection (303) between its gate electrode (294) and the first conductivity type region (Nepi) at the side of the lateral device closer to the active area (260), such that a voltage difference (function of active device in Fig. 23) between the active area (260 and the peripheral edge (edge of 267) is distributed across the lateral devices, the method comprising forming the trenches (wherein 293 and 294 are located) gate electrodes (293 and 294) and layers of gate insulating material (261) of lateral devices

in the same respective process steps (see Fig. 11-23 respectively or each of the elements for respective process steps) as trenches, insulated electrodes therein and layers of material insulating the insulated electrodes of devices in the active area (260).

With regard to claim 9, Williams shows a method semiconductor device forming a region of the first conductivity type (267) in devices of the active area (260) in the same process step (see Fig. 11-23 respectively or each of the elements for respective process steps) as the first conductivity type region (267) of the lateral devices (Fig. 23).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ELIAS M. ULLAH whose telephone number is (571)272-1415. The examiner can normally be reached on weekdays, between 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571)272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ELIAS M ULLAH/
Examiner, Art Unit 2893

/Matthew Reames/
Primary Examiner, Art Unit 2893